

LISTING OF CLAIMS

1. (Currently Amended) A CMOS imager, comprising:

a photoconversion device; and

a ~~first~~ transfer transistor, ~~having said transfer transistor comprising a transfer~~ gate with a first side and a second side opposite said first side, said transfer gate being associated with said photoconversion device at said first side of said transfer gate, ~~said first transistor also having a single active area extension region associated with said second side of said gate and a halo implant region below said single active area extension region;~~

a reset transistor at said second side of said transfer gate, said reset transistor comprising a reset gate; and

a floating diffusion region at said second side of said transfer gate, between said transfer gate and said reset gate, said floating diffusion region comprising an active area extension region at said second side of said transfer gate and a halo implant region below said active area extension region, wherein said floating diffusion region is closer to said reset gate than to said transfer gate.

2. (Cancelled).

3. (Cancelled).

4. (Currently Amended) The CMOS imager of claim 1, wherein said ~~first~~ transfer transistor has an underlying channel region, said channel region having a threshold voltage adjustment implant.

5. (Currently Amended) The CMOS imager of claim 1, wherein said ~~first~~ transfer transistor has a gate length which is ~~increased relative to~~ greater than that of all other transistors in electrical communication with said photoconversion device of a same pixel cell.

6. (Currently Amended) The CMOS imager of claim 1, wherein said halo implant region extends partially below the transfer gate ~~of said first transistor.~~

7. (Original) The CMOS imager of claim 1, wherein said photoconversion device is one of a photodiode, a photogate, or a photoconductor.

8. (Currently Amended) The CMOS imager of claim 1, wherein said ~~single~~ active area extension region and said halo implant region are laterally spaced away from the transfer gate ~~of said first transistor~~ by a portion of a substrate supporting said first transistor and including said active area extension region.

9. (Currently Amended) The CMOS imager of claim 1, wherein said photoconversion device is part of a four transistor pixel circuit comprising ~~[[a]] said~~ transfer transistor ~~as said first transistor~~, ~~[[a]]~~ said reset transistor, a source follower transistor, and a row select transistor.

10. (Original) The CMOS imager of claim 9, wherein at least one of said reset transistor and said source follower transistor have a single active area extension region.

11. (Cancelled).

12. (Cancelled).

13. (Currently Amended) The CMOS imager of claim 1, wherein said active area extension region ~~of~~ at said first transistor second side of said transfer gate has a dopant concentration of about 1×10^{12} to about 3×10^{13} ions/cm².

14. (Currently Amended) The CMOS imager of claim 1, wherein said ~~first transfer~~ transistor has a single insulating spacer, said spacer positioned on said second side of said transistor gate and over said active area extension region and said halo implant.

15. (Currently Amended) A pixel sensor cell, comprising:

a semiconductor substrate;

a transfer transistor over said substrate, said transfer transistor having a single active area extension region located on a first side of said transfer transistor;

a photosensor in electrical communication with said transfer transistor, said photosensor being within said substrate on a second side of said transfer transistor which is opposite to said first side;

a reset transistor gate over said substrate and spaced apart from said transfer transistor; and

a floating diffusion region on the first side of said transfer transistor and adjacent said reset transistor gate, said floating diffusion region being in electrical communication with said active area extension region and ~~having comprising~~ a halo implant region below said single active area extension region and an n-type doped region at the surface of said substrate and spanning said floating diffusion region and said single active area extension region.

16. (Currently Amended) The pixel sensor cell of claim 15, wherein said transfer transistor has ~~an underlying channel region, said channel region having a~~ threshold voltage adjustment implant in said substrate below a gate of said transfer transistor.

17. (Currently Amended) The pixel sensor cell of claim 15, wherein said transfer transistor has a gate length which is ~~increased relative to~~ greater than that of all other transistor gates in electrical communication with said photosensor of said pixel sensor cell.

18. (Original) The pixel sensor cell of claim 15, wherein said reset transistor comprises two active area extension regions as lightly doped drains on opposite sides of said reset transistor gate.

19. (Original) The pixel sensor cell of claim 15, wherein said reset transistor comprises a single active area extension region on a side opposite said floating diffusion region.

20. (Original) The pixel sensor cell of claim 15, further comprising at least a source follower transistor and a row select transistor.

21. (Currently Amended) A pixel sensor cell, comprising:

a semiconductor substrate;

a reset transistor over said substrate;

a photosensor in electrical communication with said reset transistor, said photosensor being within said substrate on a first side of said reset transistor;

a single active area extension region in said substrate adjacent to said reset transistor, said single active area extension region being on a side of said reset transistor which is opposite to said first side; ~~and~~

a halo implant region in said substrate below said single active area extension region; and

an n-type layer at the surface of said substrate and over said single active area extension region.

22. (Original) The pixel sensor cell of claim 21, wherein said reset transistor has an underlying channel region, said channel region having a threshold voltage adjustment implant.

23. (Withdrawn) The pixel sensor cell of claim 21, wherein said reset transistor has a gate length which is increased relative to other transistor gates in electrical communication with said photosensor.

24. (Original) The pixel sensor cell of claim 21, wherein said photosensor and said reset transistor are part of a transistor pixel circuit that further comprises a source follower transistor and a row select transistor.

25. (Original) The pixel sensor cell of claim 22, wherein said single active area extension region of said reset transistor is a lightly doped drain.

26. (Currently Amended) An image sensor, comprising:

a semiconductor substrate;

a transfer gate over said substrate;

a reset ~~transistor~~ gate over said substrate, wherein said transfer gate has a gate length greater than that of said reset transistor;

a floating diffusion region in said substrate and ~~in electrical communication with said reset transistor at a first side of~~ between said transfer gate and said reset transistor gate, said floating diffusion region being closer to said reset gate than to said transfer transistor gate;

a single active area extension region in said substrate adjacent to said ~~reset transistor~~ transfer gate and said floating diffusion region, said single active area extension region being on a second side of said reset transistor which is opposite to said first side; and

a halo implant region in said substrate below said single active area extension region;

an n-type surface layer over said floating diffusion region and said single active area extension region;

a threshold voltage implant in said substrate below said transfer gate; and

a photodiode adjacent said transfer gate at a side opposite said active area extension region and said floating diffusion region.

27. (Original) The image sensor of claim 26, wherein the image sensor is a CMOS imager.

28. (Currently Amended) The image sensor of claim ~~[[27]]~~ 26, further comprising a photodiode in electrical contact with said reset transistor, said photodiode being within said substrate on said first side of said reset transistor wherein said

floating diffusion region and said single active area extension region are laterally separated from said transfer gate in a direction toward said reset gate by a portion of said substrate.

29. (Currently Amended) The image sensor of claim [[27]] ~~26, wherein said floating diffusion region is located within a sensor array~~ further comprising a source follower gate and a row select gate.

30. (Currently Amended) The image sensor of claim [[26]] ~~29, wherein the image sensor is a CCD imager~~ at least one of said reset gate, said source follower gate, and said row select gate are associated with a second single active area extension region.

31. (Currently Amended) The image sensor of claim 29, wherein said ~~floating diffusion region is located outside a sensory array~~ transfer gate has a gate length greater than that of said source follower gate and said row select gate.

32. (Currently Amended) An imager device, comprising:

an image processor; and

a pixel array for supplying signals to said image processor, at least one pixel of said array comprising:

a photoconversion device[[,]] ; and

a first transistor gate associated with said photoconversion device at a first side of said transistor gate, said gate having a length which is greater than that of all other transistor gates of said pixel;

~~said transistor gate having~~ a single lightly doped drain on a second side of said transistor gate opposite said first side[[,]] ;

~~an underlying~~ a channel region ~~having under said transistor gate and~~
comprising a threshold voltage adjustment implant[[,]] ; and

a halo implant below said lightly doped drain, ~~and said gate also having a~~
~~length which is increased relative to other transistor gates of said pixel.~~

33. (Currently Amended) The imager device of claim 32, ~~wherein said first~~
~~transistor gate is of a reset transistor in electrical communication with said~~
~~photoconversion device~~ further comprising a surface n-type layer over said lightly
doped drain.

34. (Original) The imager device of claim 32, wherein said first transistor gate is of a transfer transistor in electrical communication with said photoconversion device.

35. (Cancelled).

36. (Cancelled).

37. (Original) The imager device of claim 32, wherein said photoconversion device is a photodiode.

38. (Currently Amended) An integrated circuit, comprising a transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region on a side of said transistor opposite from said photodiode, ~~and~~ a halo implant below said single active area extension region, an n-type layer over said single active area extension region, and a threshold voltage implant below said transistor.

39. (Currently Amended) The integrated circuit of claim 38, further comprising a ~~threshold voltage adjustment implant below~~ floating diffusion region adjacent a gate of said transistor, said single active area extension region and said halo implant being a part of said floating diffusion region.

40. (Previously Presented) The integrated circuit of claim 38, wherein said transistor has a gate length which is increased relative to any transistor gate length of other transistors of a same pixel.

41. (Currently Amended) The integrated circuit of claim 38, ~~further comprising a source/drain region adjacent to said active area extension region, wherein~~ said active area extension region and said ~~source/drain~~ floating diffusion region being are laterally spaced away from a gate of said transistor by a portion of a substrate supporting said transistor.

42. (Previously Presented) The integrated circuit of claim 38, further comprising an insulating layer over said transistor and said photodiode, said insulating layer extending to a floating diffusion region adjacent to said active area extension region.

43. (Previously Presented) The integrated circuit of claim 38, wherein said transistor and said photodiode are part of a CMOS imager pixel.

44. (Withdrawn) The integrated circuit of claim 38, wherein said transistor and said photodiode are part of a CCD imager.

45. (Previously Presented) The integrated circuit of claim 38, wherein said transistor is part of a pixel having at least two other transistors in electrical communication with said photodiode.

46. (Previously Presented) A pixel cell, comprising a transistor in electrical contact with a photodiode, said transistor comprising a single active area extension region and halo implant region on a opposite side of said transistor from said photodiode, said transistor also having a gate length which is increased relative to any other transistor gate length of transistors of a same pixel.

47. (Cancelled).

48. (Previously Presented) The pixel cell of claim 46, comprising a threshold voltage adjustment implant below a gate of said transistor.

49. (Previously Presented) The pixel cell of claim 46, comprising a source/drain region adjacent to said active area extension region, said active area extension region and said source/drain region being spaced away from a gate of said transistor by a portion of a substrate supporting said transistor.

50-93. (Cancelled).